SCALABLE SELF-ALIGNED DUAL FLOATING GATE MEMORY CELL ARRAY AND METHODS OF FORMING THE ARRAY

ABSTRACT OF THE DISCLOSURE

An integrated non-volatile memory circuit is formed by first growing a thin dielectric layer on a semiconductor substrate surface, followed by depositing a layer of conductive material such as doped polysilicon on this dielectric layer, the conductive material then being separated into rows and columns of individual floating gates. Cell source and drain diffusions in the substrate are continuously elongated across the rows. Field dielectric deposited between the rows of floating gates provides electrical isolation between the rows. Shallow trenches may be included between rows without interrupting the conductivity of the diffusions along their lengths. A deep dielectric filled trench is formed in the substrate between the array and peripheral circuits as electrical isolation. Various techniques are included that increase the field coupling area between the floating gates and a control gate. Other techniques increase the thickness of dielectric between control gates in order to decrease the field coupling between them.